University of Toronto, Department of Electrical and Computer Engineering

ECE 1387 - CAD for Digital Circuit Synthesis and Layout

September 2013

Instructor: Jason Anderson
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Pre-requisites: ECE 1388 (VLSI Design Methodology), or ECE 451 (VLSI Systems), or CSC 2410 (Algorithms in Graph Theory), or Permission of instructor. **Programming skills in C/C++**, including data structures.

Lecture: Fridays 5:00-7:00 PM in room BA 4164 (Bahen Building)

Papers/Readings: Available in PDF on course website.

Evaluation:				
	Assignments	45% (3)	Paper	25%
	Exercises	20% (3 or 4)	Class Participation	10%

Assignments: Programming implementations of CAD problems such as placement, routing, and technology mapping using optimization strategies such as simulated annealing, dynamic programming, integer linear programming (ILP), and branch and bound, and illustrated using computer graphics.

Exercises: Hands-on experience with CAD tools such as ABC (UC Berkeley), VPR (Auto Place & Route), and hMetis (Partitioning).

The Paper: A critical assessment of work in a subset of the field (chosen in consultation with the instructor) based on 3 to 4 papers.

Participation: It is the expectation that you will contribute one good question or idea per class to the general discussion. Hopefully more!

TENTATIVE Lecture and Assignment Schedule – Fall 2013

#	Date of Friday Lecture	Lecture Topic	Assignment/ Exercise Handed Out	Assignment/ Exercise Due
1	Sept 13	Introduction, Overview	Course Paper	
2	Sept 20	Routing	Assignment 1 – Routing	
3	Sept 27	Timing-Driven Routing		
4	Oct 4	Placement		Assignment 1
5	Oct 11	Placement (Analytical Techniques)	Assignment 2 – Analytical Placement	
6	Oct 18	Placement (Simulated Annealing)	Exercise 1 – VPR placement and routing	
7	Oct 25	Partitioning or SAT Solvers (Branch and Bound)	Assignment 3 – B&B as applied to partitioning or Boolean SAT	Assignment 2
8	Nov 1	Timing Analysis and Slack Allocation		Exercise 1
9	Nov 8	Partitioning (FM/Multi-Level: hMetis)	Exercise 2 – Partitioning Using hMetis or FM	Assignment 3
	Nov 15	**NO CLASS**		
10	Nov 22	Technology Mapping / Logic Synthesis (Dynamic Programming)	Exercise 3 – Technology Mapping Using Dynamic Prog in ABC (UC Berkeley)	Exercise 2
11	Nov 29	High-Level Synthsis 1	Exercise 4 – LegUp High-Level Synthesis	
12	Dec 5	High-Level Synthesis 2		Exercise 3
	Dec 20			Exercise 4
	Dec 20			Paper

NOTE: You must consult with the instructor on your paper topic by mid-November.