Jason H. Anderson, Ph.D., P.Eng

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Academic Appointments

- **University of Toronto**
  Professor of Electrical and Computer Engineering *July 2017 –*
  - Associate Department Chair, Research (2018 – 2021).
  - Jeffrey Skoll Endowed Chair in Software Engineering (2014 – 2019).
  - Faculty Affiliate of the Vector Institute for Artificial Intelligence (2018 – 2020).
  - Director of the Certificate and Minor Programs in Artificial Intelligence Engineering (2019 –).
- **University of Toronto**
  Associate Professor of Electrical and Computer Engineering (with tenure) *July 2013 – June 2017*
- **University of Toronto**
  Assistant Professor of Electrical and Computer Engineering (tenure-track) *August 2008 – June 2013*
- **University of Toronto**
  Adjunct Professor of Electrical and Computer Engineering *July 2005 – July 2008*
  - Instructor for the graduate course "ECE1387 – CAD for Digital Circuit Synthesis and Layout".
  - Adjunct faculty while working full-time in the semiconductor industry at Xilinx, Inc.

Industrial Experience

- **LegUp Computing Inc.** 2015 – present
  Chief Scientific Advisor and Co-Founder
  - Raise computational performance and energy efficiency through customized computing.
  - Ease computer hardware design through abstraction – circuit synthesis from software.
  - Start-up spawned from academic research at the University of Toronto.

- **Xilinx, Inc.** Dec. 1997 – July 2008
  Based in San Jose, California, USA for five years; based in Toronto, Canada for five and a half years

  Management Positions Held: *Principal Engineer and Manager ('07 – '08)*; *Senior Manager ('06 – '07);*
  - Two years managing all place and route activities at Xilinx, with a team of over 20 engineers.
  - Also managed and led a team of six engineers working on projects of strategic interest to Xilinx, spearheading the establishment of power-aware flows and algorithm parallelization.
  - Liaised with academia and the research community; responsible for keeping apprised of recent research results and facilitating their transfer into Xilinx.
  - Served on the Patent Committee – a select group of 10-15 technical leaders at Xilinx that reviews all company inventions and selects those which should be patented.
  - Instrumental in project planning/management, product definition, personnel management, team building and interviewing/hiring of new staff.
  - Mentored and trained many junior engineers via formal training sessions and one-on-one interactions. Well-versed in varied supervisory methods and strategies for personnel development.

Individual Contributor Positions Held: *Senior Staff Software Engineer ('04 – '06); Staff Software Engineer ('00 – '04); Senior Software Engineer ('98 – '00); Software Engineer ('97 – '98)*

- Developer and lead engineer on major projects, building state-of-the-art FPGA tools used by thousands of Xilinx customers worldwide.
- Devised, implemented and evaluated new FPGA place and route algorithms as well as enhancements to existing algorithms that led to significant reductions in tool run-time and improved quality-of-result.
- Lead developer of a post-layout optimization framework that performed incremental placement and routing to improve design performance.
- Lead developer (with one other engineer) of the Xilinx core router, based on the negotiated congestion paradigm.
- Lead developer (with one other engineer) of the Xilinx core placer, based on analytical placement techniques.
- Inventor on over 20 issued United States Patents, and also an inventor (and award recipient) of more than 10 trade secrets – patentable inventions Xilinx has chosen to keep confidential.

Education

- **University of Toronto** — Toronto, Canada
  Doctor of Philosophy (Ph.D.) in Electrical and Computer Engineering — *Sept. 2001 – June 2005*
  - Thesis: "Power optimization and prediction techniques for FPGAs".
  - Advisor: Farid N. Najm
- **University of Toronto** — Toronto, Canada
  Master of Applied Science (M.A.Sc.) in Electrical and Computer Engineering — *Sept. 1995 – Nov. 1997*
  - Thesis: "Architectures and algorithms for laser-programmed gate arrays with foldable logic blocks".
  - Advisor: Stephen D. Brown
- **University of Manitoba** — Winnipeg, Canada
  Bachelor of Science (B.Sc.) in Computer Engineering (with Distinction) — *Sept. 1991 – May 1995*
  - Thesis: "Speaker identification using artificial neural networks".
  - Advisor: Howard C. Card

Visiting Scholar Positions

- **Imperial College London** — London, UK
  Dept. of Electrical and Electronic Engineering — *Aug. – Nov. 2014*
  - Researching high-level synthesis for FPGAs, stochastic circuits.
  - Hosts: Profs. G. Constantinides and P. Cheung.
- **Tokyo Institute of Technology** — Tokyo, Japan
  Dept. of Computer and Communications Engineering — *Dec. 2014 – Mar. 2015*
  - Researching stochastic computing, lightweight embedded synthesizable processors.
  - Host: Prof. Y. Hara-Azumi.

Personal Information

- **Nationality:** Canadian.
- **Personal:** Born in Winnipeg, Canada. Traveled extensively in Canada and USA. Also traveled in Europe and Asia. Lived and worked in the San Francisco Bay Area (California, USA) for five years. Sabbatical leaves in the UK and Japan.

Research Interests

- FPGA and other programmable hardware architectures, tools, and applications, particularly computing and embedded systems applications with power and area constraints.
- Low-power design at the HDL, gate, circuit and process technology levels.
- Tools and algorithms for the automated synthesis of FPGAs and other ICs.
- VLSI architectures and circuit design.
- Software engineering for large-scale systems.

Awards and Honours

- **Best Paper Nomination at the IEEE/ACM Design Automation and Test in Europe Conf.** 2018
  - For paper: “Sensei: An Area-Reduction Advisor for FPGA High-Level Synthesis”.
- **Best Paper Award at the Int’l Conf. on Field Programmable Logic** 2017
  - For paper: “Automated Generation of Banked Memory Architectures in the High-Level Synthesis of Multi-Threaded Software”.
- **ECE Departmental Teaching Award** 2016
  - Awarded based on anonymous voting by the undergraduate students.
  - Seventh teaching award in seven successive years of undergraduate teaching.
- **Best Paper Award at the IEEE Int’l Conf. on Field-Programmable Technology** 2014
  - For paper: “Design re-use for compile time reduction in FPGA high-level synthesis flows”.
- **Fellow of the Japanese Society of the Promotion of Science (JSPS)** 2014–2015
  - Based at Tokyo Institute of Technology; Host: Prof. Y. Hara-Azumi.
- **Jeffrey Skoll Chair in Software Engineering** 2014–2019
- **Community Award at the IEEE Int’l Conf. on Field-Programmable Logic (500 euros)** 2014
  - This award is for authors who have made a significant contribution to the community by providing some material or knowledge in an open format that benefits the rest of the community.
  - Received for LegUp high-level synthesis.
- **ECE Departmental Teaching Award** 2014
- **Ontario Early Researcher Award ($140,000 over 5 years)** 2014
  - Awarded by the Ministry for Research and Innovation.
- **Best Paper Award at the ACM Int’l Symp. on FPGAs** 2014
  - For paper: “Optimizing effective interconnect capacitance for FPGA power reduction”.
- **Faculty of Applied Science and Engineering Early Career Teaching Award** 2013
- **ECE Departmental Teaching Award** 2013
  - Awarded based on anonymous voting by the undergraduate students.

- **Gordon R. Slemon Award for Excellence in the Teaching of Design ($1,000)** 2012
  - Awarded based on nominations from the undergraduate students.
- **ECE Departmental Teaching Award for ECE241 – Digital Systems** 2012
- **Paper recognized as one of the top 25 papers in first 20 years of the ACM FPGA symposium** 2012
  - For paper: “Active leakage power optimization for FPGAs” published in ACM FPGA 2004.
  - Included in the FPGA-20 special volume published by ACM in 2012.
- **Best Paper Award at the IEEE Int’l Conf. on Field Programmable Logic** 2011
  - For paper: “Reducing router run-time through algorithm and architecture”.
- **ECE Departmental Teaching Award for ECE241 – Digital Systems** 2011
- **Best Paper Nomination at the IEEE/ACM ASP-DAC Conference** 2011
  - For paper: “Area-efficient FPGA logic elements: architecture and synthesis”.
- **Best Paper Award at the IEEE Int’l Conf. on Field Programmable Technology** 2010
  - For paper: “Parallelizing FPGA placement using transactional memory”.
- **ECE Departmental Teaching Award for APS105 – Computer Fundamentals** 2010
- **ECE Departmental Teaching Award for APS105 – Computer Fundamentals** 2009
- **Nominee for the TV Ontario (TVO) Best Lecturer Competition** 2009
  - A competition held yearly in the Province of Ontario by the public broadcaster *TVO* and nominated by students.
- **Ontario Graduate Scholarship in Science and Technology ($15,000)** 2004 – 2005
- **Ontario Graduate Scholarship ($15,000)** 2003 – 2004
- **NSERC Canada Postgraduate Scholarship ($19,100 per year)** 2001 – 2003
  - Awarded (based on a national competition) by the Natural Sciences and Engineering Research Council (NSERC) of Canada to individuals pursuing doctoral studies in science or engineering.
- **Ross Freeman Award for Technical Innovation ($5,000 USD)** 2000
  - Highest innovation award given by Xilinx with 4 or 5 nominees each year and the winner chosen based on voting by the Xilinx engineering community.
  - Nominated again for Freeman award in 2001 and 2002 for different projects.
- **Software Engineering Innovation Award** 1999
  - One award given annually by Xilinx, based on peer voting within the software organization.
- **Ontario Graduate Scholarship ($15,000)** 1996 – 1997
- **IEEE Thesis Award** 1995
  - Awarded by University of Manitoba for best undergraduate thesis in Computer Engineering.
- **Sony Science Scholarship in Engineering ($1,500)** 1994 – 1995
- **Don Craik Memorial Scholarship in Engineering ($500)** 1992

Scholarly and Professional Service Activities

Service Within the University:

- **Director of the Certificate and Minor Programs in Artificial Intelligence Engineering** 2019 –
- **Associate Department Chair, Research, ECE Department** 2018 – 2021
- **Chair, Computer Engineering Research Group, ECE Department** 2015 – 2018
- **Member, Teaching Methods and Resources Committee, Faculty of Applied Science and Engr.** 2015 – present
- **Member, Advisory Council of Teaching Staff, Inst. of Leadership in Engr. Education** 2015 – present
- **Chair of the Admissions Committee, Faculty of Applied Science and Engineering** 2013 – 2014

- **Vice-Chair of the Admissions Committee, Faculty of Applied Science and Engineering** 2012 – 2013
- **Director of Undergraduate Admissions and Recruiting, ECE Department** 2012 – 2014
- **Faculty Advisor, Leaders of Tomorrow, ECE Working Group** 2011 – 2014

Journal Editorial Activities

- **Associate Editor, ACM Trans. on Reconfigurable Technology and Systems (TRETS)** 2016 –
- **Associate Editor, ACM Trans. on Design Automation of Electronic Systems (TODAES)** 2014 –
- **Associate Editor, Integration, The VLSI Journal (Elsevier)** 2011 – 2016

Conference Organizing or Executive Committee:

- **General Chair, ACM Int'l Symp. on Field-Programmable Gate Arrays (FPGA)** 2018
- **General Chair, Int'l Symp. on Highly Efficient Accelerators and Reconfig. Tech. (HEART)** 2018
- **Program Chair, ACM Int'l Symp. on Field-Programmable Gate Arrays (FPGA)** 2017
- **Technical Editor, IEEE Int'l Solid State Circuits Conference (ISSCC)** 2017
  Responsible for digital circuits and digital architectures and systems.
- **Program Co-Chair, Int'l Conf. on Field-Programmable Logic and Applications (FPL)** 2016
- **Technical Editor, IEEE Int'l Solid State Circuits Conference (ISSCC)** 2016
  Responsible for digital circuits and digital architectures and systems.
- **Track Chair, Int'l Conf. on Field-Programmable Logic and Applications (FPL)** 2015
  Responsible for Architecture and Technology Track.
- **Technical Editor, IEEE Int'l Solid State Circuits Conference (ISSCC)** 2015
  Responsible for energy-efficient and high-performance digital circuits.
- **General Chair, IEEE Int'l Conf. on Application-specific, Systems, Archs. and Proc. (ASAP)** 2015
- **Program Co-Chair, Int'l Symp. on Highly Efficient Accelerators and Reconfig. Tech. (HEART)** 2015
- **Technical Editor, IEEE Int'l Solid State Circuits Conference (ISSCC)** 2014
- **Publicity Chair, IEEE Int'l Symp. on FCCM** 2014
- **Publicity Chair, ACM Int'l Symp. on FPGAs** 2014
- **Publicity Chair, IEEE Int'l Symp. on FCCM** 2013
- **Technical Editor, IEEE Int'l Solid State Circuits Conference (ISSCC)** 2013
- **Program Co-Chairman, IEEE Int'l Conf. on Field Programmable Technology (FPT)** 2012
- **Technical Editor, IEEE Int'l Solid State Circuits Conference (ISSCC)** 2012
- **Local Arrangements Chair and Webmaster, IEEE Int'l Symp. on FCCM** 2012
- **Design Competition Chair, IEEE Int'l Conf. on Field Programmable Technology (FPT)** 2011
- **Publicity Chair, IEEE Int'l Symp. on FCCM** 2011
- **Workshop Chair, ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2009

Member of the Technical Program Committee:

- **IEEE Int'l Symposium on Field Programmable Custom Computing Machines (FCCM)** 2018
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2018
- **IEEE Int'l Conference on Application-specific Systems Architectures and Processors (ASAP)** 2017
- **Int'l Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART)** 2017
- **IEEE Int'l Symposium on Field Programmable Custom Computing Machines (FCCM)** 2017
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2017
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2017
- **Int'l Workshop on FPGAs for Software Programmers (FSP)** 2017
- **Int'l Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART)** 2016
- **IEEE Int'l Symposium on Field Programmable Custom Computing Machines (FCCM)** 2016

- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2016
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2015
- **IEEE Int'l Conference on Field Programmable Technology (FPT)** 2015
- **Int'l Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART)** 2015
- **IEEE Int'l Symposium on Field Programmable Custom Computing Machines (FCCM)** 2015
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2015
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2014
- **Int'l Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART)** 2014
- **IEEE Int'l Workshop on Logic Synthesis (IWLS)** 2014
- **IEEE/ACM Int'l Conference on Computer-Aided Design (ICCAD)** 2014
- **IEEE Reconfigurable Architectures Workshop (RAW)** 2014
- **IEEE Int'l Symposium on Field Programmable Custom Computing Machines (FCCM)** 2014
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2014
- **IEEE/ACM Int'l Conference on Computer-Aided Design (ICCAD)** 2013
- **IEEE/ACM Int'l Conference on Compilers, Architecture and Synthesis (CASES)** 2013
- **IEEE Int'l Workshop on Logic Synthesis (IWLS)** 2013
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2013
- **IEEE Int'l Conference on Field Programmable Technology (FPT)** 2013
- **IEEE Reconfigurable Architectures Workshop (RAW)** 2013
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2013
- **IEEE Int'l Symposium on Field Programmable Custom Computing Machines (FCCM)** 2013
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2012
- **IEEE Int'l Symposium on Field Programmable Custom Computing Machines (FCCM)** 2012
- **IEEE Int'l Conference on Field Programmable Technology (FPT)** 2012
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2012
- **IEEE Int'l Conference on VLSI (VLSI-SoC)** 2012
- **IEEE Reconfigurable Architectures Workshop (RAW)** 2012
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2011
- **IEEE Int'l Symposium on Field Programmable Custom Computing Machines (FCCM)** 2011
- **IEEE Int'l Conference on Field Programmable Technology (FPT)** 2011
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2011
- **IEEE Int'l Conference on VLSI (VLSI-SoC)** 2011
- **IEEE Int'l Symposium on Circuits and Systems (ISCAS) Review Committee** 2011
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2010
- **IEEE Int'l Conference on Field Programmable Technology (FPT)** 2010
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2010
- **IEEE Int'l Symposium on Circuits and Systems (ISCAS) Review Committee** 2010
- **IEEE Reconfigurable Architectures Workshop (RAW)** 2010
- **ACM Int'l Symposium on Field Programmable Gate Arrays (FPGA)** 2009
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2009
- **IEEE Reconfigurable Architectures Workshop (RAW)** 2009
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2008
- **IEEE Int'l Conference on Computer-Aided Design (ICCAD)** 2008
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2007
- **IEEE Int'l Conference on Computer-Aided Design (ICCAD)** 2007
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2006
- **IEEE Int'l Conference on Field Programmable Logic and Applications (FPL)** 2005

United States Patents

PAT1 H. Tamura, H. Fujisawa, H. Fujimoto, S. Huda, **J.H. Anderson**, “Semiconductor integrated circuit,” US Patent #9,742,405, Issued August 2017.

PAT2 H. Tamura, **J.H. Anderson**, S. Huda, H. Fujimoto, “Method for designing semiconductor integrated circuit and program,” US Patent #9,213,796, Issued December 2015.

PAT3 **J.H. Anderson**, T. Ahmed, S. Kalman, “Thread synchronization by transitioning threads to spin lock and sleep state,” US Patent #9,003,413, Issued April 2015.

PAT4 G. Jain, V. Verma, T. Ahmed, S. Kalman, S. Kwatra, C. Kingsley, **J.H. Anderson**, S. Das, “Multi-threaded deterministic router,” US Patent #8,671,379, Issued March 2014.

PAT5 G. Jain, V. Verma, T. Ahmed, S. Kalman, S. Kwatra, C. Kingsley, **J.H. Anderson**, S. Das, “Multi-threaded deterministic router,” US Patent #8,312,409, Issued November 2012.

PAT6 **J.H. Anderson**, Q. Wang, “Method of and system for generating a logic configuration for an integrated circuit,” US Patent #8,205,180, Issued June 2012.

PAT7 Q. Wang, **J.H. Anderson**, S. Gupta, “Method and apparatus for reducing clock signal power consumption within an integrated circuit,” US Patent #8,201,127, Issued June 2012.

PAT8 H. Xu, V. Verma, A. Rahut, **J.H. Anderson**, S. Kalman, “Patterns for routing nets in a programmable logic device, “ US Patent #7,797,665, Issued September 2010.

PAT9 **J.H. Anderson**, Q. Wang, “Method for technology mapping considering Boolean flexibility, “ US Patent #7,725,047, Issued June 2010.

PAT10 V. Verma, A. Rahut, S.K. Nag, **J.H. Anderson**, R. Jayaraman, “Method and apparatus for facilitating signal routing within a programmable logic device, “ US Patent #7,725,868, Issued May 2010.

PAT11 **J.H. Anderson**, M. Chirania, S. Gupta, P. Costello, “Method of reducing power of a circuit, “ US Patent #7,653,891, Issued January 2010.

PAT12 T. Jang, K. Chung, **J.H. Anderson**, Q. Wang, S. Gupta, “Method and apparatus for power optimization using don’t care conditions of configuration bits in lookup tables,” US Patent #7,603,646, Issued October 2009.

PAT13 Q. Wang, R. Aggarwal and **J.H. Anderson**, “Processing constraints in computer-aided design for integrated circuits,” US Patent #7,555,734, Issued June 2009.

PAT14 J. Saunders, K. Anandh, G. Stenz, S.K. Nag and **J.H. Anderson**, “Unified placer infrastructure,” US Patent #7,398,496, Issued July 2008.

PAT15 V. Verma, A. Rahut, S.K. Nag and **J.H. Anderson**, “Method and apparatus for facilitating signal routing within a programmable logic device,” US Patent #7,306,977, Issued December 2007.

PAT16 **J.H. Anderson**, S.K. Nag G. Stenz and S. Dasasathyan, “Method for application of network flow techniques under constraints,” US Patent #7,143,380, Issued November 2006.

PAT17 **J.H. Anderson**, S. Kalman and V. Verma, “Incremental routing in integrated circuit design,” US Patent #7,134,112, Issued November 2006.

PAT18 **J.H. Anderson**, S. Kalman and V. Verma, “Post-layout optimization in integrated circuit design,” US Patent #7,111,268, Issued September 2006.

PAT19 R. Kong and **J.H. Anderson**, “Method for computing and using future costing data in signal routing,” US Patent #7,073,155, Issued July 2006.

PAT20 **J.H. Anderson** and F.N. Najm, "Leakage power optimization for integrated circuits," US Patent #6,993,737, Issued January 2006.

PAT21 J. Saunders, K. Anandh, G. Stenz, S.K. Nag and **J.H. Anderson**, "Unified placer infrastructure," US Patent #6,983,439, Issued January 2006.

PAT22 G.-J. Nam, S. Kalman, **J.H. Anderson**, R. Jayaraman, S.K. Nag and J. Zhuang, "Method and apparatus for testing routability," US Patent #6,877,040, Issued April 2005.

PAT23 **J.H. Anderson**, "Incremental placement of design objects in an integrated circuit design," US Patent #6,871,336, Issued March 2005.

PAT24 S. Dasasathyan, G. Stenz, S.K. Nag and **J.H. Anderson**, "Placement of objects with partial shape restriction," US Patent #6,857,115, Issued February 2005.

PAT25 R. Kong and **J.H. Anderson**, "Method for computing and using future costing data in signal routing," US Patent #6,851,101, Issued February 2005.

PAT26 **J.H. Anderson**, J. Saunders, M. Chari, S. Nag and R. Jayaraman, "Method and apparatus for placement of input-output design objects into a programmable gate array," US Patent #6,625,795, Issued September 2003.

PAT27 S. Nag, K. Chaudhary, **J.H. Anderson**, M. Chari and S. Kalman, "Method and apparatus for timing-driven implementation of a circuit design," US Patent #6,484,298, Issued November 2002.

PAT28 **J.H. Anderson**, J. Saunders, M. Chari, S. Nag and R. Jayaraman, "Placement of input-output design objects into a programmable gate array supporting multiple voltage standards," US Patent #6,289,496, Issued September 2001.

Publications

Book Chapters:

B1 H. Hsiao, **J.H. Anderson**, Yuko Hara-Azumi, "Generating Stochastic Bitstreams," chapter to appear in Stochastic Computing: Techniques and Applications, Springer, 2019.

B2 A. Canis, J. Choi, B. Fort, B. Syrowik, R.L. Lian, Y.-T. Chen, H. Hsiao, J. Goeders, S. Brown, **J.H. Anderson**, "LegUp high-level synthesis," chapter in FPGAs for Software Engineers, Springer, 2016.

B3 M. Hutton, V. Betz, **J.H. Anderson**, "FPGA synthesis and physical design," chapter in Electronic Design Automation for Integrated Circuits, CRC Press, 2015.

B4 S. Huda, **J.H. Anderson**, "Circuits and architectures for low-power FPGAs," chapter in Reconfigurable Logic: Architecture, Tools and Applications, CRC Press, 2015.

Refereed Journal Publications (Published or Accepted):

P1 *J. Choi*[1], S.D. Brown, **J.H. Anderson**, "From Pthreads to multi-core hardware systems in LegUp high-level synthesis for FPGAs," accepted to appear in *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*, 2017.

P2 *S. Huda*, **J.H. Anderson**, "Leveraging unused resources for energy optimization of FPGA interconnect," accepted to appear in *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*, 2017.

P3 N. Sakamoto, T. Ahmed, **J.H. Anderson**, Y. Hara-Azumi, "Subleq: A Two-Instruction-Set Computer," *IEEE Embedded Systems Letters*, vol. 9, no. 2, June 2017.

[1]Names of students directly supervised by Prof. Anderson appear in *italics*.

P4 *C.E. LaForest*, **J.H. Anderson**, "Evaluation of Overlay, HLS, and HDL FPGA Implementations," accepted to *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, 2017.

P5 *J. Kim*, **J.H. Anderson**, "Synthesizable Standard Cell FPGA Fabrics Targetable by the Verilog-to-Routing (VTR) CAD Flow," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 10, no. 2, April 2017.

P6 P. Leong, H. Amano, **J.H. Anderson**, K. Bertels, *et al.*, "The first 25 years of the FPL conference – significant papers," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 10, no. 2, April 2017.

P7 R. Nane, V.-M. Sima, F. Ferrandi, C. Pilato, *J. Choi*, *B. Fort*, *A. Canis*, *Y.T. Chen*, *H. Hsiao*, S. Brown, **J.H. Anderson**, Koen Bertels, "A survey and evaluation of FPGA high-level synthesis tools," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 35, No. 10, pp. 1591-1604, October 2016.

P8 *S.A. Chin*, *J. Luu*, *S. Huda*, **J.H. Anderson**, "Hybrid LUT/Multiplexer FPGA Logic Architectures," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 24, No. 4, pp. 1280-1292, April 2016.

P9 *Q. Huang*, *R. Lian*, *A. Canis*, *J. Choi*, *R. Xi*, *N. Calagar*, S. Brown, **J.H. Anderson**, "The effect of compiler optimizations on high-level synthesis-generated hardware," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, Vol. 8, No. 3, 2015.

P10 *J. Luu*, G. Goeders, M. Wainberg, A. Summerville, T. Yu, K. Nasartschuk, *M. Nasr*, S. Wang, T. Liu, N. Ahmed, K. Kent, **J.H. Anderson**, J. Rose, V. Betz, "VTR 7.0: Next generation architecture and CAD system for FPGAs," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, Vol. 7, No. 2, 2014.

P11 *B. Teng*, **J.H. Anderson**, "Latch-based performance optimization for FPGAs," *IEEE Transactions on Computer Aided Design for Integrated Circuits and Systems (TCAD)*, Vol. 32, No. 5, pp. 667-680, 2013.

P12 *M. Gort*, **J.H. Anderson**, "A combined architecture/algorithm approach to reducing FPGA routing time," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 21, No. 6, pp. 667-679, 2013.

P13 *A. Canis*, *J. Choi*, *M. Aldham*, *V. Zhang*, *A. Kammoona*, T. Czajkowski, S. Brown, **J.H. Anderson**, "LegUp: Open source high-level synthesis for FPGA-based processor/accelerator systems," Vol. 13, No. 2, *ACM Transactions on Embedded Computing Systems (TECS)*, 2013. (24 page manuscript).

P14 *C. Ravishankar*, **J.H. Anderson**, A. Kennings, "FPGA power reduction by guarded evaluation considering logic architecture," *IEEE Transactions on Computer Aided Design for Integrated Circuits and Systems (TCAD)*, Vol. 31, No. 9, pp. 1305-1318, September 2012.

P15 **J.H. Anderson**, Q. Wang. *C. Ravishankar*, "Raising FPGA logic density through synthesis-inspired architecture," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 20, No. 3, pp. 537-550, March 2012.

P16 *M. Gort*, **J.H. Anderson**, "Accelerating FPGA routing through parallelization and engineering enhancements," *IEEE Transactions on Computer Aided Design for Integrated Circuits and Systems Systems (TCAD)*, Vol. 31, No. 1, pp. 61-74, January 2012.

P17 T. Ahmed, P. Kundarewich, **J.H. Anderson**, "Packing techniques for Virtex-5 FPGAs," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, Vol. 2, No. 3, September 2009.

P18 **J.H. Anderson** and F.N. Najm, "Low-power programmable FPGA routing circuitry," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 8, pp. 1048-1060, August 2009.

P19 **J.H. Anderson** and F.N. Najm, "Active leakage power optimization for FPGAs," *IEEE Transactions on Computer-Aided Design for Integrated Circuits and Systems (TCAD)*, Vol. 25, No. 3, pp. 423-437, March 2006. ****9th-most downloaded IEEE EDA article in 2006 [June 2007 newsletter of the IEEE Council on EDA (CEDA)].**

P20 **J.H. Anderson** and F.N. Najm, "Power estimation techniques for FPGAs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 12, No. 10, pp. 1015-1027, October 2004.

Refereed International Conference Publications (Accepted or Published):

P21 J. Cheng, S. Fleming, *Y.T. Chen*, **J.H. Anderson**, G. Constantinides, "EASY: Efficient Arbiter SYnthesis from Multi-threaded Code," to appear in the ACM International Symposium on Field-Programmable Gate Arrays (FPGA), to be held at Monterey, California, February, 2019.

P22 H. Sim, **J.H. Anderson**, J. Lee, "Exclusive On-Chip Memory Architecture for Energy-Efficient Deep Learning Acceleration," to appear in the IEEE/ACM Asia and Soutch Pacific Design Automation Conference (ASP-DAC), to be held at Tokyo, Japan, January 2019.

P23 *J.H. Kim*, **J.H. Anderson**, "FPGA Architecture Enhancements for Efficient BNN Implementation," to appear in the IEEE International Conference on Field-Programmable Technology (IEEE FPT), to be held at Naha, Japan, December 2018.

P24 *Kuang-Ping Niu*, **J.H. Anderson**, "Compact Area and Performance Modelling for CGRA Architecture Evaluation," to appear in the IEEE International Conference on Field-Programmable Technology (IEEE FPT), to be held at Naha, Japan, December 2018.

P25 *B. Grady*, **J.H. Anderson**, "Synthesizable Heterogeneous FPGA Fabrics," to appear in the IEEE International Conference on Field-Programmable Technology (IEEE FPT), to be held at Naha, Japan, December 2018.

P26 J. Chen, X. Liu, **J.H. Anderson**, "Software-Specified FPGA Accelerators for Elementary Functions," to appear in the IEEE International Conference on Field-Programmable Technology (IEEE FPT), to be held at Naha, Japan, December 2018.

P27 *O. Ragheb*, **J.H. Anderson**, "High-Level Synthesis of FPGA Circuits with Multiple Clock Domains," IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), Boulder, CO, April 2018.

P28 *S.A. Chin*, **J.H. Anderson**, "An Architecture-Agnostic Integer Linear Programming Approach to CGRA Mapping," IEEE/ACM Design Automation Conference (DAC), San Francisco, CA, June 2018.

P29 *H. Hsiao*, **J.H. Anderson**, "Sensei: An Area-Reduction Advisor for FPGA High-Level Synthesis," IEEE/ACM Design, Automation and Test in Europe Conference (DATE), Dresden, Germany, March 2018.

P30 *S. Bansal*, *H. Hsiao*, T. Czajkowski, **J.H. Anderson**, "High-Level Synthesis of Software-Customizable Floating-Point Cores," IEEE/ACM Design, Automation and Test in Europe Conference (DATE), Dresden, Germany, March 2018.

P31 *J. H. Kim*, *B. Grady*, *R. Lian*, J. Brothers, **J.H. Anderson**, "FPGA-Based CNN Inference Accelerator Synthesized from Multi-Threaded C Software," IEEE Int'l System-on-Chip Conference (SOCC), Munich, Germany, September, 2017.

P32 *Y.-T. Chen*, **J.H. Anderson**, "Automated Generation of Banked Memory Architectures in the High-Level Synthesis of Multi-Threaded Software," Int'l Conference on Field-Programmable Logic and Applications (FPL), Ghent, Belgium, September 2017.

P33 *S. A. Chin*, N. Sakamoto, *A. Rui*, *J. Zhao*, *J. H. Kim*, Y. Hara-Azumi, **J.H. Anderson**, "CGRA-ME: A Unified Framework for CGRA Modelling and Exploration," IEEE Int'l Conference on Application-specific Systems, Architectures and Processors (ASAP), Seattle, WA, July 2017.

P34 *J. Choi*, *R. Lian*, S. Brown, **J.H. Anderson**, "A Unified Software Approach to Specify Pipeline and Spatial Parallelism in FPGA Hardware," IEEE Int'l Conference on Application-specific Systems, Architectures and Processors (ASAP), London, UK, July 2016.

P35 *S. Huda*, **J.H. Anderson**, "Power optimization of FPGA interconnect via circuit and CAD techniques," invited paper to appear in the *ACM International Symposium on Physical Design (ISPD)*, Santa Rosa, CA, April 2016.

P36 *S. Huda*, **J.H. Anderson**, “Towards PVT-Tolerant Glitch-Free Operation in FPGAs,” *ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, to be held in Monterey, CA, February 2016 [Acceptance rate: 19%].

P37 **J.H. Anderson**, Y. Hara-Azumi, S. Yamashita, “Effect of LFSR seeding, scrambling and feedback polynomial on stochastic computing accuracy,” *ACM/IEEE Design Automation and Test in Europe Conference (DATE)*, Dresden, Germany, March 2016 [Acceptance rate: 24%].

P38 *J. Choi*, S. Brown, **J.H. Anderson**, “Resource and memory management techniques for the high-level synthesis of software threads into parallel FPGA hardware,” *IEEE Int’l Conference on Field-Programmable Technology (FPT)*, Queenstown, New Zealand, December, 2015.

P39 T. Ahmed, N. Sakamoto, **J.H. Anderson**, Y. Hara-Azumi, “Synthesizble-from-C embedded processor based on MIPS-ISA and OISC,” *IEEE Int’l Conference on Embedded and Ubiquitous Computing (EUC)*, Porto, Portugal, October, 2015.

P40 *Jin Hee Kim*, **J.H. Anderson**, ”Synthesizable FPGA fabrics targetable by the Verilog-to-Routing (VTR) CAD flow,” *Int’l Conference on Field-Programmable Logic and Applications (FPL)*, London, UK, September 2015.

P41 *S. Hadjis*, *A. Canis*, *R. Sobue*, Y. Hara-Azumi, H. Tomiyama, **J.H Anderson**, ”Profiling-driven multi-cycling in FPGA high-level synthesis,” *ACM/IEEE Design Automation and Test in Europe Conference (DATE)*, Grenoble, France, in March 2015 [Acceptance rate: 22%].

P42 *M. Gort*, **J.H. Anderson**, “Design re-use for compile time reduction in FPGA high-level synthesis flows,” *IEEE International Conference on Field-Programmable Technology (FPT)*, Shanghai, China, December 2014. (**Best Paper Award**)

P43 *C.E. LaForest*, **J.H. Anderson**, J.G. Steffan, “Approaching overhead-free execution on FPGA soft processors,” *IEEE International Conference on Field-Programmable Technology (FPT)*, Shanghai, China, December 2014.

P44 *N. Calagar*, S. Brown, **J.H. Anderson**, “Source-Level debugging for FPGA high-Level synthesis,” *IEEE International Conference on Field-Programmable Logic and Applications (FPL)*, Munich, Germany, September 2014.

P45 *A. Canis*, **J.H. Anderson**, S. Brown, “Modulo SDC scheduling with recurrence minimization in high-Level synthesis,” *IEEE International Conference on Field-Programmable Logic and Applications (FPL)*, Munich, Germany, September 2014.

P46 *B. Fort*, *A. Canis*, *J. Choi*, *N. Calagar*, *R. Lian*, *S. Hadjis*, *Y.T. Chen*, *M. Hall*, B. Syrowik, T. Czajkowski, S. Brown, **J.H. Anderson**, “Automating the Design of Processor/Accelerator Embedded Systems with LegUp High-Level Synthesis,” invited paper in the *IEEE International Conference on Embedded and Ubiquitous Computing (EUC)*, Milan, Italy, August 2014.

P47 *J. Luu*, C. McCullough, S. Wang, *S. Huda*, Y. Bo, C. Chiasson, K. Kent, **J. Anderson**, J. Rose and V. Betz, “On hard adders and carry chains in FPGAs,” *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Boston, MA, May 2014. [Acceptance rate: 16%.]

P48 *T. Diop*, N. Enright Jerger, **J.H. Anderson**, “Power modeling for heterogeneous proessors,” *ACM Workshop on General Purpose Computing with GPUs (GPGPU7)*, Salt Lake City, UT, March 2014.

P49 *S. Huda*, **J.H. Anderson**, H. Tamura, “Optimizing effective interconnect capacitance for FPGA power reduction,” *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 11-20, Monterey, CA, Febuary 2014. (**Best Paper Award**) [Acceptance rate: 19%].

P50 *J. Luu*, J. Rose, **J.H. Anderson**, “Towards interconnect-adaptive packing for FPGAs,” *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, pp. 21-31, Monterey, CA, Febuary 2014. [Acceptance rate: 19%].

P51 *J. Choi*, **J.H. Anderson**, S. Brown, “From software threads to parallel hardware in FPGA high-level synthesis,” *IEEE International Conference on Field-Programmable Technology (FPT)*, pp. 270-279, Kyoto, Japan, December 2013. [Acceptance rate: 21%]

P52 *A. Klimovic*, **J.H. Anderson**, “Bitwidth-optimized hardware accelerators with software fallback,” *IEEE International Conference on Field-Programmable Technology (FPT)*, pp. 136-143, Kyoto, Japan, December 2013. [Acceptance rate: 21%]

P53 *S. Chin*, **J.H. Anderson**, “A case for hardened multiplexers in FPGAs,” *IEEE International Conference on Field-Programmable Technology (FPT)*, pp. 42-49, Kyoto, Japan, December 2013. [Acceptance rate: 21%]

P54 *E. Mora-Sanchez*, **J.H. Anderson**, “Leakage power reduction in FPGA DSP circuits through algorithmic noise tolerance,” *IEEE International Conference on Reconfigurable Computing and FPGAs (ReConFig)*, Cancun, Mexico, December 2013.

P55 *A. Canis*, *J. Choi*, *B. Fort*, *R. Lian*, *Q. Huang*, N. Calagar, *M. Gort*, *J. Qin*, T. Czajkowski, S. Brown, **J.H. Anderson**, ”From software to accelerators with LegUp high-level synthesis,” invited paper to appear in the *IEEE/ACM International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)*, to be held at Montreal, October, 2013.

P56 *T. Diop*, *S. Gurfinkel*, **J.H. Anderson**, N. Enright Jerger, “DistCL: A framework for the distributed execution of OpenCL kernels,” *IEEE International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS)*, San Francisco, CA, August, 2013. [Acceptance rate: 27%]

P57 *S. Huda*, **J.H. Anderson**, H. Tamura, “Charge recycling for power reduction in FPGA interconnect,” *IEEE International Conference on Field-Programmable Logic and Applications (FPL)*, Porto, Portugal, September, 2013.

P58 *Q. Huang*, *R. Lian*, *A. Canis*, *J. Choi*, *R. Xi*, S. Brown, **J.H. Anderson**, “The effect of compiler optimizations on high-level synthesis for FPGAs,” *IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 89-96, Seattle, WA, 2013. [Acceptance rate: 16%]

P59 *A. Canis*, **J.H. Anderson**, S. Brown, “Multi-pumping for resource reduction in FPGA high-level synthesis,” *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, pp. 194-197, Grenoble, France, March, 2013. [Acceptance rate: 36%]

P60 *M. Gort*, **J.H. Anderson**, “Range and bitmask analysis for hardware optimization in high-level synthesis,” *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 773-779, Yokohama, Japan, 2013. [Acceptance rate: 31%]

P61 *C. Ravishankar*, A. Kennings, **J.H. Anderson**, “FPGA power reduction by guarded evaluation considering physical information,” *IEEE International Conference on Very-Large Scale Integration for Systems-on-Chip (VLSI-SoC)*, pp. 271-274, Santa Cruz, CA, October 2012.

P62 *M. Gort*, **J.H. Anderson**, “Analytical placement for heterogeneous FPGAs,” *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 143-150, Oslo, Norway, 2012. [Acceptance rate: 28%].

P63 *J. Choi*, *K. Nam*, *A. Canis*, **J.H. Anderson**, S. Brown, T. Czajkowski, “Impact of cache architecture and interface on performance and area of FPGA-based processor/parallel-accelerator systems,” *IEEE International Symposium on Field Programmable Custom Computing Machines (FCCM)*, pp. 17-24, Toronto, Canada, 2012. [Acceptance rate: 22%].

P64 Z. Poulos, Y.-S. Yang, **J.H. Anderson**, A. Veneris, B. Le, “Leveraging reconfigurability to raise productivity in FPGA functional debug,” *IEEE/ACM Design Automation and Test Conference (DATE)*, pp. 292-295, Dresden, Germany, 2012. [Acceptance rate: 34%].

P65 *S. Hadjis*, *A. Canis*, **J.H. Anderson**, *J. Choi*, *K. Nam*, S. Brown, T. Czajkowski, “Impact of FPGA architecture on resource sharing in high-level synthesis,” *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 111-114, Monterey, CA, 2012. [Acceptance rate: 41%].

P66 *W. Shum*, **J.H. Anderson**, "Analyzing and predicting the impact of CAD algorithm noise on FPGA speed performance and power," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 107-110, Monterey, CA, 2012. [Acceptance rate: 41%].

P67 J. Rose, *J. Luu*, K. Kent, C. W. Yu, O. Densmore, J. Goeders, A. Somerville, K. Kent, P. Jamieson, **J.H. Anderson**, "The VTR Project: Architecture and CAD for FPGAs from Verilog to routing," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 77-86, Monterey, CA, 2012. [Acceptance rate: 24%].

P68 *M. Aldham*, **J.H. Anderson**, S. Brown, *A. Canis*, "Low-cost hardware profiling of run-time and energy in FPGA embedded processors," *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, pp. 61-68, Santa Monica, CA, 2011. [Acceptance rate: 26%].

P69 *B. Teng*, **J.H. Anderson**, "Latch-based performance optimization for FPGAs," *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 58-63, Crete, Greece, 2011. [Acceptance rate: 28%].

P70 *M. Gort*, **J.H. Anderson**, "Reducing FPGA router run-time through algorithm and architecture," *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 336-342, Crete, Creece, 2011. (**Best Paper Award**) [Acceptance rate: 28%].

P71 *W. Shum*, **J.H. Anderson**, "FPGA glitch power analysis and reduction," *ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, pp. 27-32, Fukuoka, Japan, 2011. [Acceptance rate: 22%].

P72 *A. Canis*, *J. Choi*, *M. Aldham*, *V. Zhang*, *A. Kammoona*, **J.H. Anderson**, S. Brown, T. Czajkowski, "LegUp: High-level synthesis for FPGA-based processor/accelerator systems," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)"*, pp. 33-36, Monterey, CA, February, 2011. [Acceptance rate: 45%].

P73 *J. Luu*, **J.H. Anderson**, J. Rose, "Architecture description and packing for logic blocks with hierarchy, modes and complex interconnect," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)"*, pp. 227-236, Monterey, CA, February, 2011. [Acceptance rate: 26%].

P74 **J.H. Anderson**, Q. Wang, "Area-efficient FPGA logic elements: architecture and synthesis," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 369-375, Yokohama, Japan, January 2011. (**Nominated for Best Paper**) [Acceptance rate: 31%].

P75 *A. Rakhshanfar*, **J.H. Anderson**, "An integer programing placement approach for FPGA clock power reduction," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 831-836, Yokohama, Japan, January 2011. [Acceptance rate: 31%].

P76 *M. Gort*, **J.H. Anderson**, "Deterministic multi-core parallel routing for FPGAs," *IEEE International Conference on Field Programmable Technology (FPT)*, pp. 78-86, Beijing, China, December 2010. [Acceptance rate: 20%].

P77 S. Birk, J.G. Steffan, **J.H. Anderson**, "Parallelizing FPGA placement using transactional memory," *IEEE International Conference on Field Programmable Technology (FPT)*, pp. 61-69, Beijing, China, December 2010. (**Best Paper Award**) [Acceptance rate: 20%].

P78 **J.H. Anderson**, *C. Ravishankar*, "FPGA power reduction by guarded evaluation," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 157-166, Monterey, CA 2010. [Acceptance rate: 25%].

P79 **J.H. Anderson**, "A PUF design for secure FPGA-based embedded systems," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 1-6, Taipei, Taiwan, 2010. [Acceptance rate: 34%].

P80 **J.H. Anderson**, Q. Wang, "Improving logic density through synthesis-inspired architecture," *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 105-111, Prague, Czech Republic, 2009. [Acceptance rate: 25%].

P81 *S. Huda*, *M. Mallick*, **J.H. Anderson**, "Clock gating architectures for FPGA power reduction," *IEEE International Conference on Field Programmable Logic and Applications (FPL)*, pp. 112-118, Prague, Czech Republic, 2009. [Acceptance rate: 25%].

P82 Q. Wang, S. Gupta, **J.H. Anderson**, "Clock power reduction for Virtex-5 FPGAs," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 13-22, Monterey, CA, 2009. [Acceptance rate: 26%]

P83 T. Ahmed, P. Kundarewich, **J.H. Anderson**, B. Taylor and R. Aggarwal, "Architecture-specific packing for Virtex-5 FPGAs," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 5-13, Monterey, CA, 2008. [Acceptance rate: 29%]

P84 S. Gupta, **J.H. Anderson**, L. Farragher, Q. Wang, "CAD techniques for power optimization in Virtex-5 FPGAs," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 85-88, San Jose, CA, 2007. [Acceptance rate: 33%]

P85 **J.H. Anderson** and F.N. Najm, "Low-power programmable routing circuitry for FPGAs," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 602-609, San Jose, CA, 2004. [Acceptance rate: 24%]

P86 **J.H. Anderson** and F.N. Najm, "A novel low-power FPGA routing switch," *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 719-722, Orlando, FL, 2004. [Acceptance rate: 39%]

P87 **J.H. Anderson**, S. Nag, K. Chaudhary, S Kalman, C. Madabhushi and P. Cheng, "Run-time-conscious automatic timing-driven FPGA layout synthesis," *International Conference on Field Programmable Logic and Applications (FPL)*, pp. 168-178, Antwerp, Belgium, 2004. [Acceptance rate: 42%]

P88 **J.H. Anderson**, F.N. Najm and T. Tuan, "Active leakage power optimization for FPGAs," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 33-41, Monterey, CA, 2004. [Acceptance rate: 27%] **Selected as one of the top-20 papers in the first 20 years of ACM FPGA (2012).**

P89 **J.H. Anderson** and F.N. Najm, "Interconnect capacitance estimation for FPGAs," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 713-718, Yokohama, Japan, 2004.

P90 **J.H. Anderson** and F.N. Najm, "Switching activity analysis and pre-layout activity prediction for FPGAs," *ACM/IEEE International Workshop on System-Level Interconnect Prediction (SLIP)*, pp. 15-21, Monterey, CA, 2003.

P91 **J.H. Anderson** and F.N. Najm, "Power-aware technology mapping for LUT-based FPGAs," *IEEE International Conference on Field Programmable Technology (FPT)*, pp. 211-218, Hong Kong, 2002. [Acceptance rate: 39%]

P92 **J.H. Anderson**, J. Saunders, S. Nag, C. Madabhushi and R. Jayaraman, "A placement algorithm for FPGA designs with multiple I/O standards," *International Conference on Field Programmable Logic and Applications (FPL)*, LNCS 1896, Springer-Verlag, pp. 211-220, Villach, Austria, 2000.

P93 **J.H. Anderson** and S.D. Brown, "Technology mapping for large complex PLDs," *ACM/IEEE Design Automation Conference (DAC)*, pp. 698-703, San Francisco, CA, 1998. [Acceptance rate: 36%]

P94 **J.H. Anderson** and S.D. Brown, "An LPGA with foldable logic blocks," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, pp. 244-252, Monterey, CA, 1998.

Magazine Articles (Unrefereed), Design Competitions:

P95 *J. Cai*, *R. Lian*, *M. Wang*, *A. Canis*, *J. Choi*, *B. Fort*, *E. Miao*, *Y. Zhang*, *N. Calagar*, S. Brown, **J.H. Anderson**, "From C to Blokus Duo with LegUp High-Level Synthesis," accepted to appear in the *IEEE International Conference on Field-Programmable Technology (FPT)*, to be held at Kyoto, Japan, December 2013.

P96 S. Gupta and **J. Anderson**, "Optimizing FPGA power with ISE design tools," *Xcell Journal – The Journal for Programmable Logic Users*, Vol. 60, pp. 16-19, First Quarter 2007.

Research Impact / Citations

- **h-index (Google Scholar October 2018): 31**
- **Citations (Google Scholar October 2018): $\sim$3400**

Software Artifacts Released

- **LegUp: High-level circuit synthesis** 2011 – 2017
  - LegUp is an open source high-level synthesis tool that *automatically* compiles C program to a hybrid system comprising a processor and custom hardware accelerators. The accelerators work in tandem with the processor to execute the program on an FPGA-based platform with superior performance and energy efficiency to a software-only solution. An overarching aim of the project is to make FPGA technology accessible to software engineers.
  - The tool (freely available at `http://www.legup.org`) is one of the few open source systems of its kind and it has already been downloaded by over 5000 research groups around the world since its initial release in March 2011.

University Courses Taught

Graduate:

- **ECE1387 – CAD for Digital Circuit Synthesis and Layout** July 2005 – present
  - Course deals with algorithms for automatic circuit synthesis for digital integrated circuits, with a concentration on the back-end of the flow: technology mapping, partitioning, placement, routing, timing analysis and physical synthesis.

Undergraduate:

- **ECE253 – Digital and Computer Systems** 2017
  - A second-year course on digital design and computer organization.
- **ECE241 – Digital Systems** 2009 – 2016, 2018
  - A second-year course on digital design using Verilog and FPGAs.
- **APS105 – Computer Fundamentals** 2008 – 2015
  - A first-year introductory course on programming and problem solving in C.

Graduate Students Currently Supervised

Ph.D. Candidates:

- **Blair Fort** 2012 – present
  Topic: High-level circuit synthesis.
- **Xander Chin** 2012 – present
  Topic: FPGA architectures and circuits.
- **Jin Hee Kim** 2015 – present

Topic: FPGA architectures and circuits.

- **Joy (Yu Ting) Chen** 2017 – present
  Topic: TBD.
- **Julie Hsiao** 2017 – present
  Topic: TBD.

M.A.Sc. Candidates:

- **Brett Grady** 2016 – present
  Topic: Synthesizable FPGA fabrics.
- **Steven Niu** 2016 – present
  Topic: Coarse-grained reconfigurable arrays.
- **Ian Taras** 2017 – present
  Topic: TBD.
- **Matthew Walker** 2017 – present
  Topic: TBD.
- **Nicolas Giamblanco** 2017 – present
  Topic: TBD.

Graduate Students Previously Supervised

- **Joy Yu Ting Chen, M.A.Sc.** 2014 – 2017
  M.A.Sc. Thesis: Automated generation of banked memory architecutres in the high-level synthesis of multi-threaded software.
  Current position: Ph.D. student.
- **Julie Hsuan Hsiao, M.A.Sc.** 2014 – 2017
  M.A.Sc. Thesis: Making HLS a bit wiser: from standard high-level datatypes to arbitrary low-level bitwidths.
  Current position: Ph.D. student.
- **Safeen Huda, Ph.D.** 2012 – 2017
  Ph.D. Thesis: Circuits, architectures and CAD for low-power FPGAs.
  Current position: Efinix, Inc., Santa Clara, CA, USA.
- **James (Jongsok) Choi, Ph.D.** 2012 – 2016
  Ph.D. Thesis: From Software Threads to Parallel Hardware with LegUp High-Level Synthesis.
  Current position: LegUp Computing Inc., Toronto, ON.
- **Ruo Long (Lanny) Lian, M.A.Sc.** 2013 – 2016
  M.A.Sc. Thesis: A Framework for FPGA-Based Acceleration of Neural Network Inference with Limited Numerical Precision via High-Level Synthesis with Streaming Functionality.
  Current position: LegUp Computing Inc., Toronto, ON.
- **Jin Hee Kim, M.A.Sc.** 2013 – 2015
  Topic: Synthesizable FPGA fabrics.
  Current position: Ph.D. student.
- **Andrew Canis, Ph.D.** 2008 – 2015
  Ph.D. Thesis: LegUp High-Level Synthesis Framework
  Andrew was co-supervised by Prof. S. Brown.
  Andrew transferred from the M.A.Sc. to the Ph.D. program.
  Current position: LegUp Computing Inc., Toronto, ON.
- **Charles Eric LaForest, Ph.D.** 2013 – 2014
  Ph.D. Thesis: High-Speed Soft-Processor Architecture for FPGA Overlays.
  Current position: AMD, Markham, ON.

Eric was co-supervised by Prof. J.G. Stefan.

- **Jason Luu, Ph.D., M.A.Sc.** 2008 – 2014
  Ph.D. Thesis: Architecture-Aware Packing and CAD Infrastructure for Field-Programmable Gate Arrays.
  M.A.Sc. Thesis: A Hierarchical Description Language and Packing Algorithm for Heterogeneous FPGAs.
  Current position: Altera Corp., Toronto, ON.
  Jason was co-supervised by Prof. J. Rose.
- **Nazanin Calagar, M.A.Sc.** 2012 – 2014
  Topic: Source-Level Debugging Framework Design for FPGA High-Level Synthesis.
  Current position: Microsoft Corp., Redmond, WA, USA.
  Nazanin was co-supervised by Prof. S. Brown.
- **Steven Gurfinkel, M.A.Sc.** 2011 – 2014
  Topic: Heterogeneous CPU/GPU computing architecture.
  Current position: NVIDIA, Santa Clara, CA, USA.
  Steven was co-supervised by Prof. N. Enright Jerger.
- **Marcel Gort, Ph.D.** 2009 – 2013
  Topic: Fast CAD for FPGAs.
  Current position: Altera, Corp., Toronto, ON.
- **Tahir Diop, M.A.Sc.** 2011 – 2013
  Topic: Distributed GPU execution and heterogeneous processor power modeling.
  Current position: TXIO, Toronto, ON.
  Tahir was co-supervised by Prof. N. Enright Jerger.
- **Edgar Mora-Sanchez, M.Eng.** 2011 – 2012
  Topic: Approximate/probabilistic circuits in FPGAs.
  Current position: Intel Corp., Austin, TX, USA.
- **Jongsok Choi, M.A.Sc.** 09/2009 – 05/2012
  Thesis: Enabling Hardware/Software Co-Design in High-Level Synthesis.
  Current position: Ph.D. candidate, University of Toronto.
  James was co-supervised by Prof. S. Brown.
- **Bill Teng, M.A.Sc.** 09/2009 – 08/2011
  Thesis: Optimizing FPGA Performance Using Latches.
  Current position: Achronix Semiconductor, Santa Clara, CA, USA.
- **Warren Shum, M.A.Sc.** 09/2009 – 09/2011
  Thesis: Glitch Reduction and CAD Algorithm Noise in FPGAs.
  Current position: Altera Corporation, Toronto, ON.
- **Mark Aldham, M.A.Sc.** 09/2009 – 05/2011
  Thesis: Low-Cost Hardware Profiling of Run-Time and Energy in FPGA Soft Processors.
  Current position: Microsoft Corp., Redmond, WA, USA.
  Mark was co-supervised by Prof. S. Brown.

Visiting Graduate Students Supervised

- **Yuta Otsuka (Visiting from Tohoku University, Japan)** 05/2016 – 02/2017
- **Noriaki Sakamoto (Visiting from Tokyo Institute of Technology, Japan)** 07/2015 – 09/2015
- **Ryoya Sobue (Visiting from Ritsumeikan University, Japan)** 08/2012 – 09/2012

Undergraduate Researchers Supervised

- **Graham Hoyes (NSERC summer researcher)** Summer 2018
  Graham received an NSERC Undergraduate Summer Research Award (USRA).
- **Justin Hai (NSERC summer researcher)** Summer 2018
  Justin received an NSERC Undergraduate Summer Research Award (USRA).
- **Tristan Chen (NSERC summer researcher)** Summer 2018
  Tristan received an NSERC Undergraduate Summer Research Award (USRA).
- **Alireza Nickooie (NSERC summer researcher)** Summer 2017
  Alireza received an NSERC Undergraduate Summer Research Award (USRA).
- **Alexander Mertens (NSERC summer researcher)** Summer 2017
  Alex received an NSERC Undergraduate Summer Research Award (USRA).
- **Zakary Georgis-Yap (NSERC summer researcher)** Summer 2017
  Zak received an NSERC Undergraduate Summer Research Award (USRA).
- **Steven Shizhang Yin (ECE summer researcher)** Summer 2017
- **Samridhi Bansal (ECE summer researcher)** Summer 2017
- **James Jin (NSERC summer researcher)** Summer 2016
  Jim received an NSERC Undergraduate Summer Research Award (USRA).
- **Dhruv Chawla (NSERC summer researcher)** Summer 2016
  Jim received an NSERC Undergraduate Summer Research Award (USRA).
- **Allan Rui (NSERC summer researcher)** Summer 2016
  Jim received an NSERC Undergraduate Summer Research Award (USRA).
- **Fan Xie (NSERC summer researcher)** Summer 2016
  Jim received an NSERC Undergraduate Summer Research Award (USRA).
- **Jim Zhao (NSERC summer researcher)** Summer 2015
  Jim received an NSERC Undergraduate Summer Research Award (USRA).
- **Jenny Deng (ECE summer researcher)** Summer 2015
- **Mathew Hall (NSERC summer researcher)** Summer 2014
  Mathew received an NSERC Undergraduate Summer Research Award (USRA).
- **Emily Miao (NSERC summer researcher)** Summer 2013
  Emily received an NSERC Undergraduate Summer Research Award (USRA).
- **Yolanda Wang (ECE summer researcher)** Summer 2013
- **William Cai (NSERC summer researcher)** Summer 2013
  William received an NSERC Undergraduate Summer Research Award (USRA).
- **Yvonne Zhang (U of T summer researcher)** Summer 2013
  Yvonne received a University of Toronto Excellence Award (UTEA).
- **Ryan Xi (ECE summer researcher)** Summer 2012
  Ryan received a Faculty Undergraduate Summer Research Award.
- **Miad Nasr (NSERC summer researcher)** Summer 2012
  Miad received an NSERC Undergraduate Summer Research Award (USRA).
- **Ruo Long (Lanny) Lian (NSERC summer researcher)** Summer 2012
  Lanny received an NSERC Undergraduate Summer Research Award (USRA).
- **Qijing (Jenny) Huang (U of T summer researcher)** Summer 2012
  Jenny received a University of Toronto Excellence Award (UTEA).
- **Yifei (Alex) Liu (ECE summer researcher)** Summer 2011
  Alex received an ECE Entrance Research Award.
- **Stefan Hadjis (NSERC summer researcher)** Summer 2011
  Stefan received an NSERC Undergraduate Summer Research Award (USRA).
- **Kevin Nam (NSERC summer researcher)** Summer 2011
  Kevin received an NSERC Undergraduate Summer Research Award (USRA).

- **Ahmed Kammoona (NSERC summer researcher)** Summer 2010
  Ahmed received an NSERC Undergraduate Summer Research Award (USRA).
- **Victor Zhang (ECE summer researcher)** Summer 2010
  Victor received an ECE Entrance Research Award.
- **Chirag Ravishankar (NSERC summer researcher)** Summer 2009
  Chirag received an NSERC Undergraduate Summer Research Award (USRA).

Undergraduate Design Projects and Engineering Science Theses Supervised

- **Sirina Sit, Ramya Prasad (design project)** 2018 – 2019
- **Shuer Li, Gloria Li, Garret Li, Fanbo Meng (design project)** 2018 – 2019
- **Arash Homayouni, Andrew Choi, Peter Tanugraha, Maru Jayakumar (design project)** 2018 – 2019
- **Gokul Kaushik, Zi Chew, Hengyue Chen, Mohamed Nazeer (design project)** 2017 – 2018
- **Aya Elsayed, Angel Serah, Harshita Huria, Shraddha Buch (design project)** 2017 – 2018
- **Mathew Hall, Matthew Walker, Meghan Lele (design project)** 2016 – 2017
- **Eric Yang (Engineering Science thesis)** 2016 – 2017
- **Sherry Shi (Engineering Science thesis)** 2015 – 2016
- **Michelle Lee and Sonny Kim (design project)** 2015 – 2016
- **Danny Liu and Ang Shiuh (design project)** 2015 – 2016
- **Qijing Huang, Jack Luo, John Yan (design project)** 2014 – 2015
- **Justin Tai, Heewoo Ahn, Julie Hsiao, Wilson Feng (design project)** 2013 – 2014
- **Stefan Hadjis (Engineering Science thesis)** 2013 – 2014
- **Joy Chen (Engineering Science thesis)** 2013 – 2014
- **Ana Klimovic (Engineering Science thesis)** 2012 – 2013
- **John Qin (Engineering Science thesis)** 2012 – 2013
- **Hubert Ka, Jin-Hee Kim, Joel John (design project)** 2012 – 2013
- **Ahmed Kammoona, Victor Zhang, Bryce Long (design project)** 2012 – 2013
- **Benjamin Hare (Engineering Science thesis)** 2011 – 2012
- **Jack Fu (Engineering Science thesis)** 2011 – 2012
- **Neil Issac and Keyi Shi (design project)** 2011 – 2012
- **Anthony Hau, Gavin Lam, Juan Fuentes (design project)** 2010 – 2011
- **Karen Tam (Engineering Science thesis)** 2009 – 2010
- **Ali Rakhshanfar (Engineering Science thesis)** 2009 – 2010
- **Richelle Bernardo and Anahita Panthaky (design project)** 2009 – 2010
- **James Lee and Se-Hwan Gil (design project)** 2009 – 2010
- **Safeen Huda and Muntasir Mallick (design project)** 2008 – 2009
- **Alvin Lui and Stephan Massin (design project)** 2008 – 2009
- **Safa Mahmood (Engineering Science thesis)** 2008 – 2009

Student Supervision Summary

Ph.D. students currently supervised:	5
M.A.Sc. students currently supervised:	5
Ph.D. students graduated:	6
M.A.Sc. students graduated:	12

M.Eng. students graduated:	1
Undergraduate researchers supervised:	29
Undergraduate project/thesis students:	62

Keynotes, Invited Talks, Lectures and Short Courses Taught

- **J.H. Anderson**, *Hsuan Hsiao*, "Synthesizing FPGA Circuits from Software," invited talk at Intel Research Labs, Santa Clara, February 2018.
- **J.H. Anderson**, "A Reduced-Precision Zero-Skipping FPGA-Based CNN Inference Accelerator Synthesized from Multi-Threaded C Software," invited talk at the Symposium on Stochastic and Approximate Computing for Signal Processing and Machine Learning (part of IEEE GlobalSIP), Montreal, Canada, November 2017.
- **J.H. Anderson**, "Heterogeneous Accelerator Summer School," a one-week short course taught jointly with 6 other instructors at Harbin Institute of Technology, China, in July 2017.
- **J.H. Anderson**, "LegUp High-Level Synthesis (working title)," keynote talk at the 2016 IEEE Int'l Conference on Field-Programmable Technology (FPT), Xian, China, December 2016.
- **J.H. Anderson**, "Synthesizing Circuits from Software with LegUp High-Level Synthesis," invited talk at IBM T.J. Watson Research Lab, NY, USA, and the Hong Kong University of Science and Technology, Hong Kong, July 2016.
- **J.H. Anderson**, "Performance-aware programming with application accelerators," a one-week short course taught jointly with 5 other instructors at the University of Hong Kong, Hong Kong, July 2018, July 2016 and July 2014, sponsored by the Croucher Foundation.
- **J.H. Anderson**, "HiPEAC summer school on advanced computer architecture and compilation for high-performance and embedded systems," a one-week short course taught jointly with other instructors, Fiugi, Italy, July 2015.
- **J.H. Anderson**, "High-level synthesis for FPGAs and the LegUp open-source HLS project," keynote talk at the 2015 IEEE NASA/ESA Conference on Adaptive Hardware Systens, Montreal, June 2015.
- **J.H. Anderson**, "Overview of the LegUp FPGA high-level synthesis project, and ongoing FPGA circuits/architecture research," invited talks delivered at Fujitsu Laboratories Limited, Kawasaki, Japan, and Samsung Electronics, Suwon, Korea, in March 2015.
- **J.H. Anderson**, "CAD and Circuit Techniques for Power Optimization in FPGA Interconnect," invited talk at Tokyo Institute of Technology and Keio University, Tokyo Japan, in January and February, 2015.
- **J.H. Anderson**, "Raising Computational Throughput and Energy Efficiency by Synthesizing Software into FPGA Hardware," invited talk at Tohoku University, Sendai, Japan, January 2015.
- **J.H. Anderson** and B. Carrion Schafer, "FPGA high-level synthesis: from software to programmable hardware," tutorial delivered at the ACM/IEEE Asia-South Pacific Design Automation Conference (ASP-DAC), Tokyo, Japan, January 2015.
- **J.H. Anderson**, "LegUp High-Level Synthesis: Overview and Current Research," invited talk at Imagination Technologies, Hertfordshire, UK, November 2014.
- **J.H. Anderson**, "Raising Computational Throughput and Energy Efficiency by Synthesizing Software into FPGA Hardware," invited talk at the University of Manchester (UK) in October 2014, and the University of Cambridge (UK) in November 2014.
- **J.H. Anderson**, "LegUp high-level synthesis," invited talk at the First Int'l Workshop on FPGAs for Software Programmers (FSP), Munich, Germany, September 2014.

- **J.H. Anderson**, “Interconnect power reduction techniques for FPGAs,” EPFL, Lausanne, Switzerland, June 2014.
- **J.H. Anderson**, “LegUp: Open source high-level synthesis for FPGA-based processor/accelerator systems,” University of British Columbia, Vancouver, BC, March 2014.
- **J.H. Anderson**, “Recent research with the LegUp open-source high-level synthesis framework,” Nanyang Technological University (NTU), Singapore, March 2013.
- S. Huda, **J.H. Anderson**, “Next generation FPGA architectures and circuits,” Fujitsu Labs of America (FLA), Santa Clara, CA, February 2013.
- J. Choi, A. Canis, **J.H. Anderson**, “LegUp high-level synthesis: overview and recent research,” Xilinx, Inc., San Jose, CA, February 2013.
- **J.H. Anderson**, S. Brown, A. Canis, J. Choi, “LegUp high-level synthesis: a crash course for users and researchers,” a 2.5 hour tutorial delivered at the ACM International Symposium on Field-Programmable Gate Arrays (FPGA), Monterey, CA, February 2013.
- **J.H. Anderson**, J. Choi, “LegUp high-level synthesis for FPGA-based processor/accelerator systems,” Korean Advanced Institute for Science and Technology (KAIST), Daejeon, Korea, December 2012.
- **J.H. Anderson**, J. Choi, “Introduction to high-level synthesis and the LegUp open-source framework,” Samsung Electronics, Suwon, Korea, December 2012.
- **J.H. Anderson**, “Digital logic design with the FPGAs and the Altera DE2 board,” Ontario Computer Studies Educators Conference, Toronto, ON, November 2012.
- **J.H. Anderson**, A. Canis, “LegUp FPGA high-level synthesis: overview and approaches for resource reduction,” Intel Research Labs, Hillboro, Oregon, August 2012.
- **J.H. Anderson**, “LegUp FPGA high-level synthesis: overview and current research,” Seoul National University, Seoul, Korea, August 2012.
- J. Rose, **J.H. Anderson**, V. Betz, “Research on FPGAs at the University of Toronto,” delivered at: AMD (Austin, Texas), Altera (Austin, Texas), IBM Research (Austin, Texas), Texas Instruments (Dallas, Texas), July 2012.
- **J.H. Anderson**, “Current research activities in LegUp high-level synthesis,” Imperial College, London, UK, March 2012.
- **J.H. Anderson**, “Overview of LegUp high-level synthesis,” Achronix Semiconductor, Santa Clara, CA, February 2012.
- **J.H. Anderson**, “FPGA-based high performance computing,” Fujitsu Laboratories Ltd., Kawasaki, Japan, July 2011.
- **J.H. Anderson**, “LegUp: High-level synthesis – status and research directions,” delivered at: Ritsumeikan University (Kusatsu, Japan), and NEC Laboratories (Kawasaki, Japan), July 2011.
- **J.H. Anderson**, “LegUp: High-level synthesis – status and research directions,” University of Waterloo, Waterloo, ON, July 2011.
- **J.H. Anderson**, “LegUp: High-level synthesis for FPGA-based processor/accelerator systems,” University of Tokyo, Tokyo, Japan, January 2011.
- **J.H. Anderson**, “Graduate studies and research,” Professional Engineers Ontario Student Conference, Toronto, ON, November 2010.
- **J.H. Anderson**, “Raising FPGA logic density and energy-efficiency,” Tabula Corp, Santa Clara, CA, February 2010.

- **J.H. Anderson**, “Introduction to FPGAs and future research directions,” Fujitsu Research Labs, Kawasaki, Japan, January 2010.

Grants, Contracts and Donations

- **Huawei USA (Sole PI)** 2017 – 2018
  Total amount: $70,00.
  Average annual amount: $70,000.
  Average annual amount/PI: $70,000.
- **Samsung Electronics (sole PI)** 2016 – 2017
  Total amount: $65,000 USD.
  Annual amount: $65,000 USD.
  Annual amount/PI: $65,000 USD.
- **NSERC Collaborative Research and Development Grant (sole PI)** 2016 – 2019
  Total amount: $113,040.
  Annual amount: $37,680.
  Annual amount/PI: $37,680.
- **Huawei (co-PI w. Betz and Chow)** 2016 – 2019
  Total amount: $998,676.
  Average annual amount: $332,892.
  Average annual amount/PI: $110,964.
- **Altera Corp. (sole PI)** 2015 – 2018
  Total amount: $90,000 USD.
  Average annual amount: $30,000 USD.
  Average annual amount/PI: $30,000 USD.
- **Research Funds Attached to Jeffrey Skoll Chair (sole PI)** 2014 – 2019
  Total amount: $50,000.
  Annual amount: $10,000.
  Annual amount/PI: $10,000.
- **Ontario Early Researcher Award (sole PI)** 2014 – 2019
  Total amount: $140,000.
  Annual amount: $28,000.
  Annual amount/PI: $28,000.
- **NSERC Discovery Grant (sole PI)** 2014 – 2019
  Total amount: $155,000.
  Annual amount: $31,000.
  Annual amount/PI: $31,000.
- **NSERC Strategic Grant (co-PI w. S. Wilton [UBC])** 2013 – 2016
  Total amount: $300,000.
  Annual amount: $100,000.
  Annual amount/PI: $50,000.
- **Semiconductor Research Corporation (SRC) (co-PI w. Rose and Betz)** 2012 – 2015
  Total amount: $360,000.
  Annual amount: $120,000.
  Annual amount/PI: $40,000.
- **Fujitsu Research Labs (co-PI w. Enright Jerger and Sheikholeslami)** 2012 – 2013
  Total amount: $130,000.

Annual amount: $130,000.
Annual amount/PI: $43,333.

- **AMD Corp. and Ontario Centres of Excellence (OCE) (co-PI w. Enright Jerger)** 2012 – 2013
  Total amount: $20,000 (AMD) + $25,000 (OCE).
  Annual amount: $20,000 (AMD) + $25,000 (OCE).
  Annual amount/PI: $10,000 (AMD) + $12,500 (OCE).
- **NSERC Collaborative Research and Development Grant (lead-PI w. Brown)** 2012 – 2015
  Total amount: $127,500.
  Annual amount: $42,500.
  Annual amount/PI: $21,250.
- **Altera Equipment Grant (DE2 and DE4 FPGA Boards)** 2012
  Value: ∼$15,000.
- **Altera Corp. (co-PI w. Brown)** 2010 – 2013
  Total amount: $105,000.
  Average annual amount: $26,250.
  Average annual amount/PI: $13,125.
- **Fujitsu Research Labs (co-PI w. Enright Jerger and Sheikholeslami)** 2011 – 2012
  Total amount: $130,000.
  Annual amount: $130,000.
  Annual amount/PI: $43,333.
- **Connaught New Researcher Award (sole PI)** 2011
  Total amount: $10,000.
- **NSERC Discovery Grant (sole PI)** 2009 – 2014
  Total amount: $230,000.
  Annual amount: $46,000.
  Annual amount/PI: $46,000.
- **NSERC Engage Grant (Sponsor: AMD) (co-PI w. Enright Jerger)** 2011
  Total amount: $25,000.
  Annual amount: $25,000.
  Annual amount/PI: $12,500.
- **AMD Corp. (co-PI w. Enright Jerger)** 2011
  Total amount: $20,000.
  Annual amount: $20,000.
  Annual amount/PI: $10,000.
- **Altera Corp. (co-PI w. Brown)** 2009
  Total amount: $21,500.
  Annual amount: $21,500.
  Annual amount/PI: $10,750.
- **NSERC Collaborative Research and Development Grant (lead-PI w. Brown)** 2010 – 2011
  Total amount: $33,500.
  Annual amount: $33,500.
  Annual amount/PI: $16,750.
- **Xilinx Equipment Grant (Virtex-5 FPGA Boards)** 2009
  Value: $8,000.
- **CFI/MRI Infrastructure (Equipment) Grant (co-PI w. Tate and Enright Jerger)** 2011 – 2016
  Total amount: $582,000.
  Annual amount: $116,400.
  Annual amount/PI: $38,800.

- **Connaught New Faculty Award (sole PI)** 2008
  Total amount: $10,000.
- **University of Toronto Start-Up Funds (sole PI)** 2008
  Total amount: $100,000.

Professional Memberships and Licenses

- **Member of IEEE**
- **Member of ACM**
- **Licensed Professional Engineer (P.Eng.) in Ontario**

Interests and Activities

- **Interests:** Travel, international films, public radio, jogging, reading, learning about different ethnic foods and cultures.
- **Music:** Grade 9 Royal Conservatory of Music piano certification, music history and harmony.